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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,734	02/20/2004	Lawrence D.K.B. Dwyer	10001218-2	6626

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EXAMINER	
VU, TUAN A	
ART UNIT	**PAPER NUMBER**
2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,734	DWYER ET AL.	
	Examiner	Art Unit	
	Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7,8,10-15,17,18 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7,8,10-15,17,18 and 20-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed 2/20/2004.

As indicated in the Preliminary Amendments as of 2/20/04, claims 3, 6, 9, 19 are canceled, and claims 20-26 added. There is, however, no mention about the status of claims 16-18, and claims 7, 8 remain pending while the Amendment indicated/marked claims '6-9' as canceled. At face value, claims 1-2, 4-5, 7-8, 10-15, 20-26 are now pending for examination. The amendment is noted for the following objection.

Objected is that the sequence of claims as per the preliminary amendments is not taking under consideration the original sequence of claims so to provide deletion and addition to effect the Amendment. The sequence of claims as now submitted seemed inconsistent with that which was previously submitted, and the set of added or deleted claims appear very confusing. This is not appropriate according to the rules for making amendments, according to MPEP CFR §1.121; because what has been amended does not take effect on the very nomenclature and numerical sequence of the previous set to effectuate changes in compliance to mandatory format. It is recommended that Applicant resubmit a amended set of claims working right off (via marking changes over according to the above CFR) the exact claims initially filed as per 2/20/2004 without omitting the expression of any of one these claims, whether it be retained, amended, or deleted.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined

application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 7, 11, 20, 24 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 2, 8 of U.S. Patent No. 6,701,518 (hereinafter '518). Although the conflicting claims are not identical, they are not patentably distinct from each other because the following identified claim conflicts.

As per instant claims 1 and 11, '518 claim 1 also recites compiler 'translate first function ... second program ... having assertion instructions, ... second function ... having translated assertion instructions ... from said ... first function ... enable selective execution ...runtime input'. Although '518 claim 1 recites input in response to a failed assertion, however, the very fact of assertion use in a selective execution performed via input is reminiscent of debug based on input and would render this extra failed assertion test feature an obvious aspect of using assertion in testing as set forth by the above input-based execution.

As per instant claim 7, '518 claim 8 also recites 'to translate first function ... second program ... having assertion instructions, ... second function ... having translated assertion instructions ... from said ... first function ... enable selective execution ...runtime input' and

further 'detecting stall locations ... inserting into stall locations ... outside of said portion ... enabling selective execution ... based on run time input'.

As per instant claim 20, '518 claim 2 also recites 'translate first function ... second program ... having assertion instructions... second function ... having translated assertion instructions ... determine/detect stall locations in said second function (= machine code of first function) ... insert mode test instructions ... in said second program ... control a value ... runtime input (*analyze a mode selection input*) to execute said translated assertion code/instructions.

As per instant claim 24, '518 claim 2 also recites 'assertions instructions' from a first program to be translated into machine code (second program) and detecting stall locations in said second program, inserting mode selection instructions in said locations; and analyzing mode selection input to control based on inserted mode selection instructions.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-2, 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kolawa et al., USPN: 5,784, 553 (hereinafter Kolawa).

As per claim 1, Kolawa discloses a system for enabling selective assertion testing of computer programs based on run time inputs, comprising memory; and

a compiler (e.g. Fig. 2A), configured to translate a first function of a first program (source 11 – Fig. 2A) stored in said memory into a second function of a second program said first function having assertion instructions (e.g. source code 11, instrumented object code 22, 25– Fig. 2A), said second function having translated assertion instructions translated from (*compiler and instrumented code 25* – Fig. 2A – Note: instrumented instructions being compiled to check for instrumentation object code – see col. 7, line 22-41 – for forcing a TGS runtime linking with appropriate input reads on assertion instructions) said assertion instructions of said first function,

said compiler configured to enable selective execution of a portion (e.g. col. 5, lines 64 to col. 6, line 15; branch 256 -Fig. 18A – Note: satisfied criteria based on input for a given coverage reads on selective testing using intput/coverage as selection criteria) of said translated assertion instructions based on a run time input (e.g. input 27 – Fig 2A; see col. 9, lines 7-50).

As per claim 2, Kolawa discloses that compiler is further configured to enable the execution of each said translated assertion instruction that extends an execution time of said second function to be prevented (see Fig 2D; identify the branch condition 56 – Fig. 6A; Fig. 14 --Note: using asserted input for a selected coverage –see col. 9, lines 7-50 – discloses preventing more extensive runs to be skipped by branching to another location based on input criteria).

As per claim 11, Kolawa discloses a method for enabling selective assertion testing of computer programs based on run time inputs, comprising the steps of:

translating a first function of a first computer program into a second function of a second computer program, said first function having assertion instructions, said second function having translated assertion instructions translated from said assertion instructions of said first function (re claim 1 for corresponding rejection; Fig. 2A); and enabling selective execution of a portion of

said translated assertion instructions (e.g. col. 5, lines 64 to col. 6, line 15 – Note: satisfied criteria based on input for a given coverage reads on selective testing using intput/coverage as selection criteria) based on a run time input (e.g. input 27 – Fig 2A; see col. 9, lines 7-50).

As per claim 12, refer to claim 2.

As per claim 13, Kolawa discloses that said enabling step is automatically performed along with said translating step (e.g. col. 20-67 – instrumented Java bytecodes – see instrumented 232 – Fig. 16 -- to enable symbolic executing based on a set of input reads on enabling performed with bytecode symbolic translation and execution).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made

7. Claims 4-5, 7-8, 10, 14-15, 20, 24-26 are rejected under 35 U.S.C. 102(a) as being unpatentable over Kolawa et al., USPN: 5,784, 553, in view of Kalafatis et al., USPubN: 2003/0023834(hereinafter Kalafatis).

As per claim 4, Kolawa does not that said compiler is further configured to detect stall locations in said second function and to insert into said stall locations each said translated assertion instruction that is outside of said portion. However, Kolawa's instrumenter is disclosed as looking for identifying points at which to insert instrumentation whereby all input are used and no errors are unfound (see col. 24 line 58 to col. 25 line 58) and Java garbage collection to

salvage runtime resources (col. 17, lines 54-64). The resolving of branch locations based on instrumentation of code to check what path would fulfill criteria by Kolawa's (see Fig. 6A, 13, 18A) is suggestive that no resource should be extraneously taken by a compiler with full support, as indicated in judiciously choosing of instrumentation points (see col 17, line 66 to col. 18, line 55) to address errors (via exception) in multi threaded JVM execution. Alleviating resources in terms of minimizing instruction fetching latency, improper branch path taken leading to said exceptions and/or cache miss was a known concept at the time the invention was made; and allotting instrumentation by means of check code asserted at points unused by multithreaded runtime was one of approach contributing to Kolawa's endeavor to salvage wasted resources as taught above. According to which, Kalafatis teaches multi-threaded environment where long latency can be alleviated, and judiciously insertion of instruction to force a thread switch to prevent a resource violation analogous to assertion code by Kolawa to prevent Java exception with possibility to assert on thread flow(para 0056-0057, pg. 5; para 0093-0094, pg. 9); further, Kalafatis swith-on-idle logic (para 0059, pg. 9) in order to provide this assertion during idle time of threads. It would be obvious for one skill in the art to support the compiler by Kolawa with judicious instrumentation points at which to assert a code checking for potential resources conflict while addressing branch optimizing; and to utilize Kalafatis's approach to assert while idle (inserting assertion code where else in the multi-thread execution a idle or stall time/location occurs). One skill in the art would be motivated to do so to enable Kolawa's JVM runtime with compiler intelligence to make use of all resources, and not leave any unused bandwidth wasted when JVM runtime require maximizing error prevention and minimizing

memory loss, as analyzed above with suggestion leading to how Kalafatis usage of idle time can support Kolawa's multi-thread JVM fault-free execution endeavor.

As per claim 5, Kolawa (in view of Kalafatis) discloses said compiler is further configured to enable execution of each said translated assertion instruction that is outside of said portion (Fig. 16 - Note: asserted instruction by Kalafatis in Java runtime inherently dictates forcing of the switch regardless of the run time input as taught by Kolawa's input files – see Fig 5, 6A, 9).

As per claim 7, Kolawa discloses method for enabling selective assertion testing of computer programs based on run time inputs, comprising the steps of: translating a first function of a first computer program into a second function of a second computer program, said first function having assertion instructions, said second function having translated assertion instructions translated from said assertion instructions of said first function (refer to claim 1); inserting a block of said translated assertion instructions into said second function; and enabling selective execution of said block of translated assertion instructions based on a run time input (refer to claim 1).

Kolawa does not explicitly disclose *detecting stall locations within said second function of said second computer program; inserting one of said translated assertion instructions into one of said stall locations in response to a detection of said one stall location in said detecting step; inserting a block of said translated assertion instructions into said second function; and enabling selective execution of said block of translated assertion instructions based on a run time input.*

But this stall locations limitation to enforce a assertion checking code has been addressed in claim 4.

As per claim 8, refer to claim 5

As per claim 10, Kolawa discloses (in view of Kalafatis) enabling execution of each said translated assertion instruction that is outside of said block of translated assertion instructions (an forced switch of thread context by Kalafatis regardless of what input files is used – see claim 4 – reads on assertion regardess said run time input by Kolawa's).

As per claims 14-15, refer to the corresponding rationale as set forth in claims 4-5.

As per claim 20, Kolawa discloses a software testing system, comprising memory;

a compiler configured to translate source code into machine code, said source code stored in said memory and comprising one or more assertion instructions and said machine code stored in said memory and comprising one or more instructions representative of said source code, said mode test instructions configured to analyze a mode selection input and execute assertion handling code based upon said mode selection input (refer to corresponding rejection of claim 1); and a processor configured to request said mode selection input when said processor executes said machine code (e.g. decision module 484 – Fig. 22).

But Kolawa does not explicitly teach:

the compiler further configured to determine stall locations that occur during execution of said machine code and insert assertion instructions into said stall locations for execution, said compiler further configured to insert mode test instructions into said machine code, said mode test instructions configured to analyze a mode selection input and execute assertion handling code based upon said mode selection input; and a processor configured to request said mode selection input when said processor executes said machine code.

But this stall locations limitation to enforce a assertion checking code has been addressed in claim 4.

As per claim 24, Kolawa discloses a software testing method, comprising:

translating source code into machine code, said source code comprising one or more assertion instructions and said machine code comprising one or more instructions representative of said source code; inserting mode test instructions into said machine code, said mode test instructions

configured to analyze a mode selection input; and analyzing said mode selection input based on said mode test instructions; all of which having been addressed in claim 20.

But Kolawa does not explicitly disclose:

determining stall locations that occur during execution of said machine code;inserting assertion instructions into said stall locations for execution; inserting mode test instructions into said machine code, said mode test instructions configured to analyze a mode selection input; and analyzing said mode selection input based on said mode test instructions.

But this stall locations limitation to enforce a assertion checking code has been addressed in claim 4.

As per claim 25, Kolawa discloses mode selection input from a user via a display device (col. 5, line 653 to col 6, line 3 Note: *declarative* programming of source code to yield coverage inputs being looked for by instrumentation of source code reads on user providing selection input via a display interface).

As per claim 26, Kolawa discloses executing said assertion handling code based upon said mode selection input from said analyzing step (see Fig 18, 6A, 21-22).

Allowable subject matter

8. Claim 21 contains otherwise allowable subject matter and but is objected to because it depends on a rejected base claim. The matter deemed allowable is:

... mode selection input indicates that the assertion handling code is to be executed upon detection by said mode test instructions of a failure in said machine code.

Claims 22-23, depending on claim 21, also contain allowable subject matter.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

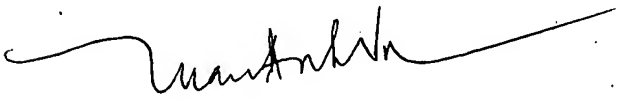
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan A Vu
Patent Examiner,
Art Unit 2193
March 04, 2007